Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) An embeddable flash memory system for non-volatile storage of code, data, and bit-streams for embedded FPGA configurations and having a modular memory array structure with N memory blocks or modules, wherein a power block, including charge pumps, is shared among different flash memory modules through a power management arbiter (PMA) block, the system comprising a single chip on which the system is integrated together with a microprocessor, said PMA block including an order block configured to order requests for the memory blocks according to a status of the request (already active or new request) and priority information.

2. (Previously Presented) The embeddable flash memory system of claim 1, comprising three different access ports, each for a specific function:

a code port to manage application code and optimized for random access time and the application system;

a data port to manage application data and for access to modify application data; and,

a floating programmable gate array (FPGA) port to manage embedded FPGA (e-FPGA) and offering a serial access for a fast download of bit streams for embedded FPGA configurations.

3. (Canceled)

4. (Previously Presented) The embeddable flash memory system of claim 1, comprising a switch block managing the requests of the memory blocks based on the output of said order block; a request decoder block configured to enable the required high voltage resources while a corresponding pump driver block manages a power down/stand-by timeout and limits requests for each resource to a maximum allowed.

5. (Previously Presented) The embeddable flash memory system of claim 2 wherein said code port comprises four configuration registers defining its addressable memory space: two at the application level, and two at the flash memory modules level.

6. (Previously Presented) The embeddable flash memory system of claim 2 wherein said second data port manages application data stored in the memory blocks using an SRAM page buffer configured to enable the application to exchange data in burst mode at maximum speed to increase performance during write operation.

7. (Previously Presented) The embeddable flash memory system of claim 2 wherein said third port comprises four configuration registers replicating information stored in said code port that is used to write e-FPGA configurations data.

8. (Previously Presented) The embeddable flash memory system of claim 2 wherein said third port uses a chip select to access addressable memory space and a burst enable to enable burst serial access.

9. (Previously Presented) The embeddable flash memory system of claim 1 wherein a testability circuits (DFT) block is provided and connected to all relevant internal signals for first internal testing and then all internally generated voltages and currents system testability; said DFT block coupled to an external high voltage power supply, and two analog input-output (IO) pads configured to provide access from external test equipment.

10.-26. (Canceled)

27. (Previously Presented) An embeddable flash memory system, comprising a non-volatile memory for non-volatile storage of code, data, and bit-streams for embedded floating programmable gate array (FPGA) configurations, the system integrated into a single chip together with a microprocessor and having a modular array structure comprising a plurality of memory blocks, wherein a power block comprising charge pumps is shared among different flash memory modules through a power management arbiter (PMA), the PMA block having an order block configured to order requests for the memory blocks in accordance with status of the request (already active or new request) and priority information; and the system further including a switch block managing the requests of the memory blocks based on the output of the order block; a request decoder block configured to enable the required high voltage resources while a corresponding pump driver block manages a power down/stand-by timeout and limits requests for each resource to a maximum allowed.

28. (Previously Presented) The embeddable flash memory system of claim 27, comprising three different access ports, each for a specific function:

a code port optimized for random access time and the application system;

a data port for access to modify application data; and,

an FPGA port offering a serial access for a fast download of bit streams for embedded FPGA configurations, wherein the code port comprises four configuration registers defining its addressable memory space: two at the application level, and two at the flash memory modules level.

29. (Previously Presented) The embeddable flash memory system of claim 28 wherein the code port comprises four configuration registers defining its addressable memory space: two at the application level, and two at the flash memory modules level.

30. (Previously Presented) The embeddable flash memory system of claim 28 wherein the data port manages application data stored in the memory blocks using an SRAM page buffer configured to enable the application to exchange data in burst mode at maximum speed to increase performance during write operation.

31. (Previously Presented) The embeddable flash memory system of claim 28 wherein the FPGA port comprises four configuration registers replicating information stored in the code port that is used to write e-FPGA configurations data.

32. (Previously Presented) The embeddable flash memory system of claim 28 wherein the FPGA port uses a chip select to access addressable memory space and a burst enable to enable burst serial access.

33. (Previously Presented) The embeddable flash memory system of claim 27 wherein a testability circuits (DFT) block connected to all relevant internal signals for first internal testing and then all internally generated voltages and currents system testability; the DFT block coupled to an external high voltage power supply, and two analog input-output (IO) pads configured to provide access from external test equipment.

34.-40. (Canceled)